

REMARKS

III. Objection to The Claim

As assumed by the Examiner, the abbreviation “LUN” refers to “logical unit”.
The text “LUN (logical unit)” has been added into paragraph [0078] so that the term
5 “LUN” in claim 17 is supported. No new matter is entered. Removal of the objection
to the claim 17 is respectfully requested.

IV. Double Patenting

Claims 1-44 and 83-94 of the instant applicant are provisionally rejected under
10 the judicially created doctrine of obviousness-type double patenting as being
unpatentable over claim 1 of copending Application 10/707,871 (hereinafter called the
reference 871).

Claim 1 of the claimed invention is directed to a computer system comprising:
a host entity for issuing IO requests; an external JBOD emulation controller coupled
15 to the host entity for emulating IO operations in response to the IO requests; and a set
of at least one physical storage device coupled to the JBOD emulation controller each
through a point-to-point serial-signal interconnect for providing storage to the
computer system through the JBOD emulation controller, wherein said JBOD
emulation controller is capable of defining at least one logical media unit (LMU)
20 comprising sections of at least one of the physical storage devices and bringing
the LMU on line or taking the LMU off line while the JBOD emulation controller
is on line. In contrast, the reference 871 is directed to a storage virtualization
computer system comprising: a host entity for issuing IO requests; an external storage
virtualization controller coupled to said host entity for executing IO operations in
25 response to said IO requests; and at least one physical storage device (PSD), each
coupled to the storage virtualization controller through a point-to-point serial-signal
interconnect, for providing storage to the storage virtualization computer system
through the storage virtualization controller. In this way, clearly, the reference 871 is
different from the claimed invention in that said JBOD emulation controller is
30 capable of defining at least one logical media unit (LMU) comprising sections of

at least one of the physical storage devices and bringing the LMU on line or taking the LMU off line while the JBOD emulation controller is on line. Since these two patent applications are quite different, the claimed subject matter in the instant application is not fully disclosed in the reference 871, and would not be 5 covered by reference 871 granted on the copending application. Therefore, no double patenting should be raised between the reference 871 and the instant application. Because claim 1 of the instant application does not have double patenting issue in view of reference 871, dependent claims 2 and 4 of the instant application that depend on the claim 1 are believed not to have double patenting issue as well.

10 Accordingly, applicants respectfully request that the rejections under the judicially created doctrine of obviousness-type double patenting be withdrawn.

V. Rejection Based On Prior Art

Claim Rejections under 35 U.S.C. §102

15 Claims 1, 2, 4-9, 11-17, 24-29, 31-35, 38-40, 44, 83, 84, and 86-93 are rejected under 35 U.S.C. § 102(e) as being anticipated by Bicknell et al. (US pub 2003/0193776).

20 The Federal Circuit reiterated that “a rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference.” In re Paulsen, 31 USPQ 2d 1671 (Fed. Cir. 1994).

Point 3 in OA

25 All the limitations of original claim 4 are merged into claim 1, and all the limitations of original claim 12 are merged into claim 8. Claims 4 and 12 are correspondingly canceled, and the dependency in the preamble of claim 5 is correspondingly amended. No new matter is entered.

30 In this way, currently amended claim 1 of the instant application claims “A computer system comprising: a host entity for issuing IO requests; an external JBOD emulation controller coupled to the host entity for emulating IO operations in response to the IO requests; and a set of at least one physical storage device coupled to the

JBOD emulation controller each through a point-to-point serial-signal interconnect for providing storage to the computer system through the JBOD emulation controller, wherein said JBOD emulation controller is capable of defining at least one logical media unit (LMU) comprising sections of at least one of the physical storage devices 5 and bringing the LMU on line or taking the LMU off line while the JBOD emulation controller is on line; and wherein said external JBOD emulation controller comprises a central processing circuitry for performing said IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.” (emphasis added)

15 Claim 8 of the instant application claims “A JBOD subsystem for providing storage to a host entity, comprising: at least one external JBOD emulation controller for coupling to the host entity for emulating IO operations in response to IO requests issued from the host entity; and a set of at least one physical storage device each coupled to the JBOD emulation controller through a point-to-point serial-signal 20 interconnect for providing storage to the host entity through the JBOD emulation controller, wherein said JBOD emulation controller is capable of defining at least one logical media unit (LMU) comprising sections of at least one of the physical storage devices and bringing a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line; and wherein said external JBOD emulation controller comprises a central processing circuitry for performing said IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device

interconnect controller for coupling to a said at least one physical storage device.” (emphasis added)

Claim 11 of the instant application claims “wherein a said at least one LMU comprises sections of a plurality of the physical storage devices.”

5 In contrast, Bicknell only discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100”, but fails to disclose “wherein said external JBOD emulation controller comprises a central processing circuitry for performing said IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.”

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15 Bicknell neither discloses nor suggests the “said external JBOD emulation controller comprising a central processing circuitry (CPC) for performing IO operation in response to said IO requests of said host entity” as claimed in the present invention.

20 Bicknell discloses a disc storage subsystem 100 comprising a pair controllers 108, an intermediate electronic component 110, a midplane card 112, and a plurality of disc drives 106 (See paragraph [0016]). In operation, a host computer may access data stored in the disc drives 106 through controllers 108 and the intermediate electronic components 110. Each intermediate electronic component 110 determines which controller 108 is provided data access to a particular disc drive 106 by opening and closing data communication paths between the disc drive 106 and each of the controllers 108. In the event that one of the controllers 108 fails, data stored in the disc drives 106 can still be accessed by the host computer through the remaining active controller 108 (See paragraph [0017]). Each intermediate electronic component 110 includes multiplexing electronics (MUX) 208 that operates to selectively open and close data communication paths linking data interface 144 of a disc drive 106 to each

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of the controllers 108 (See paragraph [0027]). MUX 208 includes a micro-computer 222 that monitors the control signals and controls the opening and closing of data paths 212 and 213 in response thereto. In accordance with another embodiment of the invention, micro-computer 222 of MUX 208 produces a status signal output 224 that 5 is directed to each of the controllers 108 to inform controllers 108 whether the first data path 212 or second data path 213 is open (See fig. 8 and paragraph [0028]).

In short, Bicknell discloses that a pair of storage controllers 108 both may be connected to the same host, and that both controllers 108 are connected to the same disc drive 106 through a MUX 108, in which the first and second controllers 108.1 and 108.2 are connected to the MUX 108 through a first path 212 and a second 213, and then the MUX 108 is connected to the disc drive 106. A micro-computer 222 is provided in the MUX 108 to monitor the control signals and control the opening and closing of data paths 212 and 213. The micro-computer 222 is not provided for performing IO operation in response to the IO requests of the host entity. Instead, the micro-computer 222 is provided for selectively opening or closing the paths 212 and 213. From aforesaid viewpoint, because the micro-computer 222 is used to selectively open or close the paths 212 and 213 in the MUX 108, the micro-computer 222 has to be provided in the MUX 108, and thus cannot correspond to the central processing circuitry (CPC) of the external storage virtualization controller (SVC) of the present invention. In addition, the micro-computer 222 is not provided in the controller 108. Moreover, if the micro-computer 222 were to be installed in one of the controllers 108.1 or 108.2, then the micro-computer would not be able to monitor the control signals and controls the opening and closing of data paths 212 and 213.

Therefore, applicant respectfully asserts that Bicknell neither discloses nor suggests “the central processing circuitry (CPC) for performing IO operation in response to said IO requests of said host entity” included in the external storage virtualization controller.

Additionally, Bicknell discloses an interface 200 and ports (fig.8) for connecting 30 to the MUX 208 and then to disc drive 106; i.e., Bicknell discloses “a device-side IO

device interconnect port.” **Bicknell’s patent application, however, neither discloses nor teaches “at least one host-side IO device interconnect port provided in a said at least one IO device interconnect for coupling to said host entity, in which the at least one IO device interconnect controller is coupled to said CPC.”**

5 In conclusion, applicant points out that Bicknell et al. neither disclose nor suggest at least the following features of the present invention as claimed in claim 1:

- “an external JBOD emulation controller”
- “wherein said external JBOD emulation controller comprises: a central processing circuitry (CPC) for performing said IO operations in response to said IO requests of 10 said host entity”

“at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity, in which the at least one IO device interconnect controller is coupled to said CPC.”

15 **In addition, applicants respectfully emphasizes that the present invention relates to “bring a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line” function of the present invention, which is not disclosed in Bicknell’s patent application.**

20 Take the following for example 1, when a JBOD subsystem, e.g., JBOD 1, comprising a JBOD emulation controller and 8 hot-swappable HDDs (HDD1 to HDD8), in which the HDD1 to HDD7 are defined as LMU 1 of RAID 3 level, where the HDD1 to 25 HDD6 are used to store user’s data, and HDD7 is used to store parity data, and the HDD8 is a spare HDD.

In view of aforesaid descriptions, while the JBOD emulation controller is on line, then

25 (1) when only one of the HDDs, for example, HDD2 is removed from the LMU1, the LMU1 is still on line, because there are redundant data to keep LMU1 on line.

(2) when three HDDs, for example, HDD3, HDD4, and HDD5 are removed from the LMU1 at the same time, the LMU1 is not on line any more for the host to 30 access, because RAID 3 subsystem allows only one HDD off line at the same time,

while keeping the subsystem on line for host to access.

(3) when HDD 6 fails and the system enters a degraded mode, which means that failure of any further HDD is not allowed any more for the LMU 1 to be accessed by the host before the system recovers from the degraded mode back to the normal mode, if the spare HDD8 is pre-determined to be used as a substitute for a failed HDD in the LMU1, then removing and insertion of the HDDs is not needed for the LMU1 to recover from the degraded mode to normal mode.

(4) when HDDs 4, 5 & 6 fail at the same time and the system enters an off-line mode, which means that LMU 1 is not allowed to be accessed by the host, even if there is one spare HDD, HDD8, pre-determined to be used as a substitute for a failed HDD in the LMU1, then removing or insertion of the HDDs has nothing to do with the recovery of LMU1 from the off-line mode to the normal mode.

Therefore, according to above examples, the present invention may comprise a JBOD emulation controller wherein when the JBOD emulation controller is on line, and disk drive(s) is (are) removed, the LMU 1 either could be disturbed, such as in the above case (2), or could be not disturbed, such as in the above cases (1) and (3). And what's more, when there is no disk drive removed/inserted, but the disk drive(s) fail(s), the LMU 1 could still be taken off line, such as in the above case (4).

Take the following for example 2, when a JBOD subsystem, e.g., JBOD 2, comprising a JBOD emulation controller and 8 hot-swappable HDDs (HDD1 to HDD8), but the HDD5 and HDD6 are not inserted into the subsystem, which means that there are 6 HDDs (HDD1 to HDD4 and HDD7 to HDD8, wherein HDD7 to HDD8 are spare HDDs) are inserted into the subsystem before the system is initialized, while the HDD5 and HDD6 have not been inserted into the subsystem yet.

It is assumed that the LMU2 is defined as an N-RAID (or Non-RAID) of 6 HDDs and comprises the 6HDDs, HDD1 to HDD6, wherein HDD5 and HDD6 have not been inserted into the subsystem yet, after subsystem is initialized, and data are stored therein in a sequence according to the above sequence of the HDDs. Therefore, data are stored in the HDDs in the sequence of HDD1, then HDD2, and then HDD3 and finally HDD4. Assume that the LMU2 is pre-determined to be brought on line, if at least 50% HDDs, i.e.,

3HDDs, are available for the host to access.

In view of aforesaid descriptions, while the JBOD emulation controller is on line, then:

(5) when only one of the HDDs, e.g., HDD4 is removed from the LMU2, the 5 LMU2 is still on line for the host to access data therein, if HDD4 does not have data stored therein yet, since there are still 3 HDDs (HDD1 to HDD3) to keep the LMU2 on line.

(6) if the fifth HDD is originally defined as HDD5, then when the HDD5 is 10 inserted into JBOD 2, the HDD5 will be added into the LMU2, and the LMU2 is still on line, since there are enough HDDs (HDD1 to HDD5) to keep the LMU2 on line.

(7) when 4 HDDs (over 50% of 6HDDs), e.g., HDD 1 to HDD4 are removed from the LMU2, the LMU2 is not on line any more for the host to access, since there are only two HDD left, which is not enough HDDs for the subsystem to be on line.

(8) when 4 HDDs, e.g., HDD 1 to HDD4, fail and thus over 50% of 6HDDs 15 are not available to the host to access, and the system enters an off-line mode, which means that LMU 2 is not allowed to be accessed by the host, even if there are two spare HDDs, HDD7 and HDD8, pre-determined to be used as substitutes for failed HDDs in the LMU2, then removing and insertion of the HDDs has nothing to do with the recovery of LMU2 from the off-line mode to the normal mode.

20 Therefore, according to above examples, the present invention may comprise a JBOD emulation controller wherein when the JBOD emulation controller is on line, and disk drive(s) is(are) removed/inserted, the LMU 2 either could be disturbed, such as in the above case (7), or could be not disturbed, such as in the above cases (5) and (6). And what's more, when there is no disk drive removed/inserted, but disk drive(s) 25 fail(s), the LMU 2 could still be taken off line, such as in the above case (8).

Therefore, according to the above cases (1) through (8) of the examples 1 & 2, it can be understood that insertion/removal of a disk drive into/from the subsystem has nothing to do with the "bring a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line" function of the 30 present invention.

In contrast, Bicknell discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100,” which means that what Bicknell discloses is not the same as what is recited in the claimed invention.

Besides, Bicknell only discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100,” but fails to disclose detailed descriptions regarding how to achieve **“Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100.”**

For at least these reasons, applicant asserts that currently amended claim 1 should be found allowable with respect to the teachings of Bicknell et al. Because the amended claims 1, 8 and 11 of the instant application include the same or equivalent features, applicant asserts they too should be found allowable for at least the same reasons as those provided above for amended claim 1. All claims which are dependent upon base claims 1 and 8, respectively should therefore be allowable with respect to the teachings of Bicknell et al. for at least the same reasons.

Point 6 in the OA

As per dependent claim 5, the instant application claims wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port; on the contrary, paragraph 0019 of Bicknell only discloses a redundancy system 100, but fails to disclose that said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port, and fails to host-side IO device interconnect port.

25 Point 7 in the OA

As per dependent claim 6, the instant application claims further comprising a second external JBOD emulation controller coupled to the host entity for emulating said IO operations in response to the IO requests, wherein said external JBOD emulation controller and said second external JBOD emulation controller are configured into a redundant pair, and said LMU is allowed to be brought on line or

taken off line while the JBOD emulation controller is on line; on the contrary, Fig.6, paragraph 0029, 0019 of Bicknell only discloses controller 1 and controller 2, **but fails to disclose the controllers 1 and 2 are configured into a redundant pair, and fails to disclose detailed descriptions regarding how to achieve that “disc drive 5 106 can preferable be removed without disturbing the operation of subsystem 100” as explained in point 3. Please refer to point 3.**

Point 8 in the OA

As per claim 7, the instant application claims wherein said LMU can be 10 redundantly presented to the host by both of said external JBOD emulation controllers; on the contrary, paragraph 0037 of Bicknell only discloses first and second controllers (108.1 and 108.2), **but fails to disclose disc drive assembly (104) is redundantly presented to the host by said first and second controllers.**

15 Point 9 in the OA

As per claims 13, 86 and 89, the instant application claims comprising auto-on-lining mechanism to automatically bring on line a said LMU which was previously off-line once a requisite quorum of said PSDs comes on-line, in which the auto-on-lining mechanism is used to make said LMU come on-line once a requisite 20 quorum of said PSDs comes on-line; on the contrary, **paragraph 0030 of Bicknell does not disclose the auto-on-lining mechanism at all, and thus fails to disclose to “make said LMU come on-line once a requisite quorum of said PSDs comes on-line”.**

25 Point 11 in the OA

As per claims 14, 87 and 90, the instant application claims comprising auto-off-lining mechanism to automatically take off line a said LMU which was previously on-line once a requisite quorum of said PSDs becomes off-line, in which the auto-off-lining mechanism is used to make said LMU come off-line once a 30 requisite quorum of said PSDs comes off-line; on the contrary, **paragraph 0019 of**

Bicknell only discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100”, but fails to disclose such an auto-off-lining mechanism, and thus fails to disclose to automatically take off line a said LMU once a requisite quorum of said PSDs becomes off-line.

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Point 12 in the OA

As per claim 15, the instant application claims comprising determining mechanism for automatically determining when a PSD has been removed or when one has been inserted; on the contrary, paragraph 0019 of Bicknell only disclose “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100”, but fails to disclose such a determining mechanism for automatically determining when a PSD has been removed or when one has been inserted.

15 **Point 13 in the OA**

As per claim 16, the instant application claims comprising scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD; on the contrary, paragraph 0003 of Bicknell only discloses “an electrical connection with the midplane card for data communication with the disc drives”, but fails to disclose such a scanning-in mechanism, and thus fails to disclose to automatically scan in PSDs on detection of insertion of the PSD.

Point 14 in the OA

As per claim 17, the instant application claims comprising information mechanism for informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed; on the contrary, paragraph 0017 of Bicknell only discloses “data stored in the disc drives 106 can still be accessed by the host computer through the remaining active controller 108. In this manner, the reliability of disc storage subsystem 100 is improved.”, but fails to disclose such a information mechanism for informing the host entity when the mapping of said

LMUs to host-side interconnect LUNs has changed.

Point 16 in the OA

As per claim 25, the instant application claims wherein a host-side port of said first JBOD emulation controller and a host-side port of said second JBOD emulation controller are configured into a complementary port pair; on the contrary, paragraph 0017 of Bicknell does not disclose the host-side port at all, and thus fails to disclose to configure the host-side port of said second JBOD emulation controller are configured into a complementary port pair.

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Point 17 in the OA

As per claim 26, the instant application claims wherein said complementary port pair are interconnected onto a same host-side IO device interconnect; on the contrary, Fig.6 of Bicknell does not disclose host-side IO device interconnect at all, and thus fails to disclose said complementary port pair are interconnected onto a same host-side IO device interconnect.

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Point 18 in the OA

As per claim 27, the instant application claims wherein said complementary port pair are interconnected together with switch circuitry; on the contrary, midplane card 112 of fig. 6 of Bicknell neither discloses the complementary which are interconnected onto a same host-side IO device interconnect, nor discloses the switch circuitry.

25 **Point 19 in the OA**

As per claim 28, the instant application claims wherein each port of said complementary port pair is interconnected onto a different host-side IO device interconnect; on the contrary, fig.6 of Bicknell only discloses data ports (204), but neither discloses said complementary port pair nor discloses said different host-side IO device interconnect, and thus fails to disclose that "each port of said

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complementary port pair is interconnected onto a different host-side IO device interconnect”.

Point 21 in the OA

5 As per claim 31, the instant application claims wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port; on the contrary, **fig. 6 and paragraph 0037 of Bicknell only disclose the first and second controllers each include a data port(such as 204.11 and 204.12), but fails to disclose wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port.**

10 **the host entity on more than one host-side IO device interconnect port.**

Point 22 in the OA

As per claim 32, the instant application claims comprising an enclosure management services (EMS) mechanism, in which the EMS mechanism is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. and can be interrogated by a host for these statuses (please refer to specification of the present invention; on the contrary, **paragraph 0037 of Bicknell only discloses “the multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220), but fails to disclose, such as power supplies, fans, temperatures, etc.**

15 **control signal (such as 218 or 220), but fails to disclose, such as power supplies, fans, temperatures, etc.**

20 **control signal (such as 218 or 220), but fails to disclose, such as power supplies, fans, temperatures, etc.**

Point 23 in the OA

As per claim 33, the instant application claims wherein said EMS mechanism is of a direct-connect EMS configuration; on the contrary, **fig. 8 of Bicknell does not disclose such a EMS mechanism at all, and thus fails to disclose that said EMS mechanism is of a direct-connect EMS configuration.**

25 **disclose such a EMS mechanism at all, and thus fails to disclose that said EMS mechanism is of a direct-connect EMS configuration.**

Point 24 in the OA

30 As per claim 34, the instant application claims wherein said EMS mechanism

is of a device-forward EMS configuration; on the contrary, **fig. 8 of Bicknell does not disclose such a EMS mechanism at all, and thus fails to disclose that said EMS mechanism is of a device-forward EMS configuration.**

5 **Point 25 in the OA**

As per claim 35, the instant application claims wherein said EMS mechanism implements both direct-connect and device-forward EMS configurations; on the contrary, **fig. 8 of Bicknell neither discloses said EMS mechanism nor discloses direct-connect and device-forward EMS configuration, and thus fails to disclose that said EMS mechanism implements both direct-connect and device-forward EMS configurations.**

Point 26 in the OA

As per claim 38, the instant application claims wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode; on the contrary, **paragraph 0030 of Bicknell only discloses fiber channel connectors, but fails to disclose Fibre Channel supporting point-to-point connectivity in target mode.**

20 **Point 27 in the OA**

As per claim 39 and 91, the instant application claims wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode; on the contrary, paragraph **0032 and fig.6 of Bicknell only discloses fiber channel connectors, but fails to disclose wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode.**

Point 28 in the OA

As per claim 40, the instant application claims wherein at least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in

target mode; on the contrary, paragraph 0030 and fig. 6 of Bicknell only disclose **fiber channel connectors, but fails to disclose Fibre Channel supporting private loop connectivity in target mode.**

5 **Point 30 in the OA**

All the limitations of original claim 12 are merged into claim 83 and into claim 92.
No new matter is entered.

After aforesaid merge, as per claim 83, the instant application claims “A method
10 for performing JBOD emulation in a computer system having at least one external
JBOD emulation controller and a set of at least one physical storage device connected
to the JBOD emulation controller, the method comprising: defining at least one logical
media unit (LMU) comprising sections of said set of at least one of the physical
storage device by the JBOD emulation controller; receiving and parsing IO requests
15 from a host entity by the JBOD emulation controller to perform an IO operation to
access the LMU by accessing said set of at least one of the physical storage device
through at least one device-side IO device interconnect port in point-to-point serial
signal transmission; and, while the JBOD emulation controller is on line, bringing on
line a said at least one logical media unit which is not on line or taking off line a said
20 at least one logical media unit which is on line; **and wherein said external JBOD**
emulation controller comprises a central processing circuitry for performing said
IO operation in response to said IO requests of said host entity; at least one IO
device interconnect controller coupled to said central processing circuitry; at
least one host-side IO device interconnect port provided in a said at least one IO
25 **device interconnect controller for coupling to said host entity; and at least one**
device-side IO device interconnect port provided in a said at least one IO device
interconnect controller for coupling to a said at least one physical storage
device.” (emphasis added)

30 As per claim 88, the instant application claims “wherein said at least one LMU

comprises sections of a plurality of the physical storage devices.”

As per claim 92, the instant application claims “A computer-readable storage medium having a computer program code stored therein that is capable of causing a 5 computer system having an external JBOD emulation controller and a set of at least one physical storage device connected to the JBOD emulation controller to perform the steps of: defining at least one logical medium unit comprising sections of at least one of the physical storage devices by the JBOD emulation controller; and receiving and parsing IO requests from a host entity by the JBOD emulation controller to 10 perform an IO operation to access the logical media unit (LMU) by accessing said set of at least one physical storage device through at least one device-side IO device interconnect in point-to-point serial signal transmission, wherein said JBOD emulation controller is capable of performing one of the followings while being on line: bringing on line a said at least one LMU which is not on line and taking off line a said at least one LMU which is on line; **and wherein said external JBOD emulation controller comprises a central processing circuitry for performing said IO operation in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.**” (emphasis added)

On the contrary, Bicknell only discloses “Disc drive 106 can preferably be 25 removed without disturbing the operation of subsystem 100.”, **but fails to disclose wherein said external JBOD emulation controller comprises a central processing circuitry for performing said IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling**

to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.”

5 Bicknell neither discloses nor suggests the “said external JBOD emulation controller comprising a central processing circuitry (CPC) for performing IO operation in response to said IO requests of said host entity” as claimed in the present invention.

10 Bicknell discloses a disc storage subsystem 100 comprising a pair controllers 108, an intermediate electronic component 110, a midplane card 112, and a plurality of disc drives 106 (See paragraph [0016] and Fig.6). In operation, a host computer may access data stored in the disc drives 106 through controllers 108 and the intermediate electronic components 110. Each intermediate electronic component 110 determines which controller 108 is provided data access to a particular disc drive 106 by opening and closing data communication paths between the disc drive 106 and each of the controllers 108. In the event that one of the controllers 108 fails, data stored in the disc drives 106 can still be accessed by the host computer through the remaining active controller 108 (See paragraph [0017]). Each intermediate electronic component 110 includes multiplexing electronics (MUX) 208 that operates to selectively open and close data communication paths linking data interface 144 of a disc drive 106 to each 15 of the controllers 108 (See paragraph [0027]). MUX 208 includes a micro-computer 222 that monitors the control signals and controls the opening and closing of data paths 212 and 213 in response thereto. In accordance with another embodiment of the invention, micro-computer 222 of MUX 208 produces a status signal output 224 that is directed to each of the controllers 108 to inform controllers 108 whether the first 20 data path 212 or second data path 213 is open (See fig. 8 and paragraph [0028]).
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30 In short, Bicknell disclosed that a pair storage controllers 108 both may be connected to the same host, and that both controllers 108 are connected to the same disc drive 106 through a MUX 108, in which the first and second controllers 108.1 and 108.2 are connected to the MUX 108 through a first path 212 and a second 213, and then the MUX 108 is connected to the disc drive 106. A micro-computer 222 is

provided in the MUX 108 to monitor the control signals and control the opening and closing of data paths 212 and 213. The micro-computer 222 is not provided for performing IO operation in response to the IO requests of the host entity. Instead, the micro-computer 222 is provided for selectively opening or closing the paths 212 and 213. From aforesaid viewpoint, because the micro-computer 222 is used to selectively open or close the paths 212 and 213 in the MUX 108, the micro-computer 222 has to be provided in the MUX 108, and thus cannot correspond to the central processing circuitry (CPC) of the external storage virtualization controller (SVC) of the present invention. In addition, the micro-computer 222 is not provided in the controller 108. Moreover, if the micro-computer 222 were to be installed in one of the controllers 108.1 or 108.2, then the micro-computer would not be able to monitor the control signals and controls the opening and closing of data paths 212 and 213.

Therefore, applicant respectfully asserts that Bicknell neither discloses nor suggests “the central processing circuitry (CPC) for performing IO operation in response to said IO requests of said host entity” included in the external storage virtualization controller.

Additionally, Bicknell discloses an interface 200 and ports (fig.8) for connecting to the MUX 208 and then to disc drive 106; i.e., Bicknell discloses “a device-side IO device interconnect port.” Bicknell’s patent application, however, neither discloses nor teaches “at least one host-side IO device interconnect port provided in a said at least one IO device interconnect for coupling to said host entity, in which the at least one IO device interconnect controller is coupled to said CPC.”

In conclusion, applicant points out that Bicknell et al. neither disclose nor suggest at least the following features of the present invention as claimed in claim 1:

- “an external JBOD emulation controller”
- “wherein said external JBOD emulation controller comprises: a central processing circuitry (CPC) for performing said IO operations in response to said IO requests of said host entity”

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“at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity, in which the at least one IO device interconnect controller is coupled to said CPC.”

5 **In addition, applicants respectfully emphasizes that the present invention relates to “bring a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line” function of the present invention, which is not disclosed in Bicknell’s patent application.**

10 Take the above cases (1) through (8) of examples 1 and 2 as examples, the present invention may comprise a JBOD emulation controller wherein when the JBOD emulation controller is on line, and disk drive(s) is(are) removed/inserted, the LMU either could be disturbed, such as in the above cases (2) and (7), or could be not disturbed, such as in the above cases (1), (3), (5) and (6). And what’s more, when there is no disk drive removed/inserted, but disk drive(s) fail(s), the LMU could still be taken off line, such as in the above cases (4) and (8).

15 Therefore, according to the above cases (1) through (8) of the examples 1 & 2, it can be understood that insertion/removal of a disk drive into/from the subsystem has nothing to do with the “bring a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line” function of the present invention.

20 In contrast, Bicknell discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100,” which means that what Bicknell discloses is not the same as what is recited in the claimed invention.

25 Besides, Bicknell only discloses “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100,” but fails to disclose detailed descriptions regarding how to achieve “Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100.”

30 For at least these reasons, applicant asserts that currently amended claim 1 should be found allowable with respect to the teachings of Bicknell et al. Because the amended claims 83 and 92 of the instant application include the same or equivalent features, applicant asserts they too should be found allowable for at least the same reasons as those

provided above for amended claim s 83 and 92. All claims which are dependent upon base claims 83 and 92, respectively should therefore be allowable with respect to the teachings of Bicknell et al. for at least the same reasons.

5 **Claim rejection 35USC 103**

Point 33 in the OA

As per claims 3, 10, 41, 43, 85 and 94, the instant application claims that the point-to-point serial—signal interconnect is a serial ATA (SAS) IO device interconnect. On the contrary, col.16, line 49 of Rabinovitz and paragraph [0030] of Bicknell only 10 disclose a SCSI in a storage virtualization subsystem, but fail to disclose or teach SAS.

Point 37 in the OA

As per claim 18, the instant application claims comprising unique ID 15 determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem; on the contrary, paragraph [0114] of Watanable and Bicknell only disclose that each volume is also assigned a unique ID 1104a-c, but fail to disclose or teach such a unique ID determination mechanism for uniquely identifying said PSDs independent of their location in which they 20 are installed in the JBOD subsystem.

Point 38 in the OA

As per claim 19, the instant application claims wherein information used to uniquely identify each of said PSDs is stored on the PSD; on the contrary, paragraph 25 [0114] of Watanable and Bicknell only disclose each volume is also assigned a unique ID 1104a-c, but fails to disclose or teach that information used to uniquely identify each of said PSDs is stored on the PSD.

Point 39 in the OA

30 As per claim 20, the instant application claims wherein LMU identification and

configuration information is stored on the member PSDs that compose the LMU; on the contrary, paragraph [0114] of Watanable only discloses each volume is also assigned a unique ID 1104a-c, but fails to disclose or teach that LMU identification and configuration information is stored on the member PSDs that compose the LMU.

5 LMU.

Point 40 in the OA

As per claims 21 and 30, the instant application claims wherein LMU identification information presented to the host entity is generated from said LMU identification information stored on the member PSDs that compose the LMU, and claims further comprising ID generation mechanism to automatically generate the LMU identification information presented to the host entity when a need arises; on the contrary, paragraph [0114] of Watanable and Bicknell only disclose each volume is also assigned a unique ID 1104a-c, but fails to disclose or teach that LMU identification information presented to the host entity is generated from said LMU identification information stored on the member PSDs that compose the LMU, and fails to disclose or teach claims further comprising ID generation mechanism to automatically generate the LMU identification information presented to the host entity.

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Point 41 in the OA

As per claim 22, the instant application claims wherein LMU identification information presented to the host entity is generated from information stored in a non-volatile memory in the JBOD emulation controller; on the contrary, paragraphs [0065][0114] of Watanable and Bicknell only disclose that input, intermediate or resulting data or functional elements can further reside more transitionally or more persistently in a storage media, cache or other volatile or non-volatile memory, (e.g. storage device 307 or memory 308) in accordance with a particular application, and only disclose that each volume is also assigned a unique ID 1104a-c, for example a WWN reference for fiber channel, a SCSI name for iSCSI, and so on, but Watanable

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and Bicknell both fail to disclose wherein LMU identification information presented to the host entity is generated from information stored in a non-volatile memory in the JBOD emulation controller.

5 **Point 42 in the OA**

As per claim 23, the instant application claims wherein LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information of the member PSDs and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible; on the contrary, paragraphs [0065][0114] of Watanable and Bicknell only disclose that input, intermediate or resulting data or functional elements can further reside more transitionally or more persistently in a storage media, cache or other volatile or non-volatile memory, (e.g. storage device 307 or memory 308) in accordance with a particular application, and only disclose that each volume is also assigned a unique ID 1104a-c, for example a WWN reference for fiber channel, a SCSI name for iSCSI, and so on, but Watanable and Bicknell both fail to disclose or teach that LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information of the member PSDs and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible.

Point 44 in the OA

25 As per claim 42, the instant application claims wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode; on the contrary, fig. 11 and paragraph [1487] of Colton and Bicknell only disclose that the Sun server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance, but fail to disclose or teach that at least one said host-side IO device interconnect port is ethernet supporting the

iSCSI protocol operating in target mode.

In addition, it should be noted that field of the invention of Colton is far away from that of the present invention, in which Abstract of Colton describes that the present invention enables a multi-wavelength band to be maintained as an optical signal through only a band switch, and provides a switch node with expandable capacity for switching data optically. That is, the field of the invention of Colton is totally different from that of the present invention, in which the present invention relates to RAID system while Colton relates to a multi-wavelength band to be maintained as an optical signal through only a band switch, both of which are totally different from each other.

Prior art of Record

With regard to other prior art made of record in the Office Action, none disclose or teach the claimed invention.

15

CONCLUSION

In light of the above remarks, all objections and rejections having been addressed, and it is respectfully submitted that the present application is in a condition 20 for allowance and a Notice to that effect is earnestly solicited. If there are any remaining issues to be resolved, the applicant requests that the Examiner contact the undersigned attorney for a telephone interview.

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Sincerely yours,

Winston Hsu

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)